Amendments to the Claims

1. (CURRENTLY AMENDED) A device, comprising:

a power insulated gate field effect transistor, having main cells ~~(2)~~ controlled by a main cell insulated gate and sense cells ~~(4)~~ controlled by a sense cell insulated gate;

a sample and hold circuit ~~(10,50)~~ connected in series with the sense cells ~~(4)~~ and arranged to operate in a plurality of states including at least one sample state and a hold state;

wherein the sample and hold circuit ~~(10,50)~~ is arranged to sense the current flowing through the sense cells ~~(4)~~ when in the at least one sample state but not in the hold state.

2. (CURRENTLY AMENDED) A device according to claim 1 wherein the sample and hold circuit ~~(10)~~ is a feedback sample and hold circuit connected to the sense cells ~~(4)~~ and arranged to operate in the sample state to sense the current passing through the sense cells and having an output ~~(22)~~ arranged to drive the sense cell ~~(4)~~ gate towards a voltage in which a target current passes through the sense cells ~~(4)~~, and to operate in the hold state to hold its output voltage and to drive the main cell ~~(2)~~ insulated gate with that output voltage.

3. (CURRENTLY AMENDED) A device according to claim 2 wherein the output ~~(16)~~ of the feedback sample and hold circuit is connected to a gate drive node ~~(22)~~ connected to the sense cell ~~(4)~~ insulated gate and connected to the main cell ~~(2)~~ insulated gate through a first switch ~~(24)~~, the first switch ~~(24)~~ being held open in the sample state to isolate the main cell ~~(2)~~ insulated gate from the gate drive node ~~(22)~~ and closed in the hold state to drive the main cell ~~(2)~~ insulated gate from the gate drive node ~~(22)~~.

4. (CURRENTLY AMENDED) A device according to claim 3 wherein the feedback sample and hold circuit include comprises:

a sample and hold voltage amplifier ~~(20)~~ connected to drive the gate drive node ~~(22)~~;

an input summing node ~~(28)~~ connected to the input of the voltage amplifier ~~(20)~~;

a current supply ~~(30)~~ supplying a reference current to the input summing node ~~(28)~~; and

a current mirror circuit ~~(32)~~ connected to the input summing node ~~(28)~~, the current mirror circuit ~~(32)~~ being arranged in the sample state to pass a mirror current from the input summing node ~~(28)~~ mirroring the current passing through the sense cells ~~(4)~~;

wherein the current mirror circuit ~~(32)~~ and sample and hold voltage amplifier ~~(20)~~ are arranged to act in the sample state as a feedback loop to tend to drive the gate drive node ~~(22)~~ towards a voltage in which a target current matching the reference current passes through the sense cells ~~(4)~~.

5. (CURRENTLY AMENDED) A device according to claim 4 comprising:

source and drain output terminals ~~(6,8)~~, the main cells ~~(2)~~ being connected between the source and drain output terminals ~~(6,8)~~;

and a second switch ~~(34)~~ connected between the sense cells ~~(4)~~ and one of the source or drain output terminals ~~(6,8)~~, the circuit being arranged to open the second switch ~~(34)~~ in the sample mode and close the second switch ~~(34)~~ in the hold state to provide a current path for current passing through the sense cells ~~(4)~~ in the hold mode that does not pass through the current mirror circuit ~~(32)~~.

6. (CURRENTLY AMENDED) A device according to ~~claim 4 or 5~~ claim 4 wherein the current mirror includes:

a mirror summing node ~~(38)~~ connected to the source of the sense cells;

a current sink field effect transistor (FET) ~~(42)~~ connected to the mirror summing node ~~(38)~~ to sink the current passing through the sense cells ~~(4)~~ in the sample state;

a summing node amplifier ~~(36)~~ with an amplifier input connected to the mirror summing node ~~(38)~~ and an amplifier output connected to the gate of the current sink FET ~~(42)~~ through a third switch ~~(44,62)~~ , the third switch ~~(44,62)~~ being closed in the or each sample state;

a current mirror FET ~~(40)~~ mirroring the current sink FET ~~(42)~~, the

output of the summing node amplifier ~~(36)~~ connecting to the gate of the current mirror FET ~~(40)~~ to control the current mirror FET ~~(40)~~ to mirror the current passing through the current sink FET ~~(42)~~.

7. (CURRENTLY AMENDED) A device according to claim 6 further comprising a fourth switch ~~(46)~~ connected to the gate of the current sink FET ~~(42)~~ to switch off the current sink FET ~~(42)~~ in the hold mode.

8. (CURRENTLY AMENDED) A device according to ~~claim 6 or 7~~ claim 6 further comprising a measurement sample and hold circuit ~~(50)~~ including a measurement mirror' FET ~~(52)~~ connected to the current sink FET ~~(42)~~,

the measurement mirror FET ~~(52)~~ being connected to a mirror current output terminal ~~(58)~~,

the measurement sample and hold circuit ~~(50)~~ being arranged to operate in a measurement sample state with the second switch ~~(34)~~ open to mirror the current passing through the current sink FET ~~(42)~~ on the measurement mirror FET ~~(52)~~.

9. (CURRENTLY AMENDED) A device according to ~~claim 6 or 7~~ claim 6 wherein the current supply is pulsed to operate only in the or each sample state; the third switch ~~(62)~~ is provided between the summing node amplifier ~~(36)~~ and a common node ~~(61)~~ ; and

the gates of the mirror FET ~~(40)~~ and the current sink FET ~~(52)~~ are connected to the common node ~~(61)~~;

the device further comprising auto-zero circuitry ~~(63)~~ for zeroing the summing node amplifier ~~(36)~~ during the hold state.

10. (CURRENTLY AMENDED) A device according to claim 9, further comprising a measurement mirror FET ~~(52)~~ having a gate connected to the common node ~~(61)~~ wherein the circuit is arranged to have a measurement sample state in which a second switch ~~(34)~~ is open and current passing through the sense cells is mirrored on the measurement mirror FET ~~(52)~~.

11. (CURRENTLY AMENDED) A device according to ~~any of claims 3 to~~

~~10~~claim 3 further comprising a charge pumped current sink connected to the current mirror circuit to sink the current passing through the mirror.

12. (CURRENTLY AMENDED) A device according to claim 1 wherein the sample and hold circuit includes a current mirror circuit including:

a mirror summing node ~~(38)~~ connected to the source of the sense cells;

a current sink field effect transistor (FET) ~~(42)~~ connected to the summing node to sink the current passing through the sense cells in the or each sample mode;

a summing node sample and hold amplifier ~~(36,56)~~ with an amplifier input connected to the mirror summing node ~~(38)~~ and an amplifier output connected to the gate of the current sink FET ~~(42)~~ through a third switch ~~(44,54,62)~~, the third switch ~~(44,54,62)~~ being closed in at least one sample state to control the current sink; and

at least one mirror FET mirroring the current sink FET, the output of the summing node amplifier connecting to the gate of the mirror FET to control the mirror FET to mirror in the mirror FET the current passing in the current sink FET in a sample state.

13. (CURRENTLY AMENDED) A device according to claim 12 wherein the at least one mirror FET includes a measurement mirror FET ~~(52)~~ connected to a measurement output terminal ~~(58)~~, and the at least one sample state includes a measurement sample state in which the current on the sense cells is mirrored on the measurement output terminal ~~(58)~~.

14. (CURRENTLY AMENDED) A device according to ~~claim 12 or 13~~claim 12 wherein the at least one mirror FET includes a current mirror FET ~~(40)~~ connected to a feedback sample and hold amplifier ~~(20)~~ connected to drive the gate of the sense cells ~~(4)~~ and connected through a first switch ~~(24)~~ to drive the gate of the main cells in the hold mode.

15. (CURRENTLY AMENDED) A device according to claim 14 further comprising a current source ~~(30)~~ sourcing current into a voltage drive node ~~(28)~~ connected to an input of the feedback sample and hold amplifier ~~(20)~~, the voltage drive node ~~(28)~~ connected through the current mirror FET ~~(40)~~ to a current sink ~~(12)~~.

16. (CURRENTLY AMENDED) A device according to ~~any preceding claim~~claim 1 further comprising

control circuitry connected to control the switch or switches for cycling between the sample and the hold modes with a duty cycle in which the ratio of time in

the sample mode to time in the hold mode is in the range 1:5 to 1:50.

17. (CURRENTLY AMENDED) A method of operating a field effect transistor, including

providing a power field effect transistor having main cells ~~(2)~~ controlled

by main cell insulated gates and sense cells ~~(4)~~ controlled by sense cell insulated gates, and a sample and hold circuit ~~(10,50)~~ connected to the sense cells;

switching to at least one sample state in which the sample and hold circuit outputs a voltage to drive the sense cells but not the main cells, and sensing the sense cell current;

switching to a hold state in which the sense cell current is not measured; and

cycling between the sample and hold states.

18. (CURRENTLY AMENDED) A method of operating a field effect transistor according to claim 17 wherein the sample and hold circuit is a feedback sample and hold circuit ~~(10, 50)~~ connected to the sense cells ~~(4)~~;

in a feedback sample state, the feedback sample and hold circuit ~~(10, 50)~~ outputs a voltage to drive the sense cells ~~(4)~~ but not the main cells ~~(2)~~, the feedback sample and hold circuit output voltage being driven towards a voltage in which a predetermined target current passes through the sense cells ~~(4)~~; and

in the hold state the output voltage of the feedback sample and hold circuit is held constant and used to drive the main cell insulated gates ~~(2)~~ with the voltage.

19. (CURRENTLY AMENDED) A method of operating a field effect transistor according to ~~claim 17 or 18~~claim 17, wherein

in a measurement sample state, the sample and hold circuit ~~(50)~~ outputs a current on a measurement output terminal ~~(58)~~ corresponding to the current through the sense cells.

20. (CURRENTLY AMENDED) A method according to ~~any of claims 17 to 19~~claim 17 wherein the ratio of the time in the at least one sample state to time in the hold state is in the range 1:5 to 1:20.